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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/273,560	03/22/1999	TAKUMI HASEGAWA	Q53743	7269

7590 04/07/2004

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EXAMINER	
THANGAVELU, KANDASAMY	
ART UNIT	**PAPER NUMBER**
2123	21

DATE MAILED: 04/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/273,560	HASEGAWA, TAKUMI	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 March 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is in response to the Applicants' Amendment dated January 23, 2004. Claims 1-4 were amended. Claims 1-4 of the application are pending in the application. This office action is made final.

Response to Amendments

2. Applicant's arguments filed on January 23, 2004 have been fully considered. Claim rejections under 35 USC 112 First paragraph and 112 Second Paragraph are withdrawn in response to applicant's amendments. Response to Applicant's arguments filed on January 23, 2004, regarding art rejections under 35 U.S.C. 103 (a) is provided at Paragraph 7 below.

Drawings

3. The drawings submitted on March 22, 1999 are accepted.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Blinne et al. (BL)** (U.S. Patent 5,274,568) in view of **Hasegawa (HAS)** (U.S. Patent 6,041,168) and further in view of **Hasegawa (HS)** (U.S. Patent 5,528,511).

6.1 Claims 1 and 2 are directed to a delay analysis system; claim 3 is directed to a delay analysis method; and claim 4 is directed to a computer readable medium having a program implementing the delay analysis method. All claims are directed to making a delay analysis of a logic circuit comprising:

the system having a delay analysis library comprising connection information, delay time information for circuits and logical operation information;

the logical operation information representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit;

the delay information for the circuit based upon a logical state transition at an input terminal and its corresponding logical state transition at an output terminal as represented by the logical operation information for the circuit;

when making a delay analysis of the logic circuit comprising the at least one circuit, a delay time is selected from the delay time information according to the type of logical state transitions present at selected input and output terminals of the at least one circuit.

Therefore, claims 1-4 are rejected using the same prior art.

BL teaches method of estimating logic cell delay time. Specifically, as per Claim 1, **BL** teaches the delay analysis system for making a delay analysis of a logic circuit (Col 1, Lines 7-13);

the system having a delay analysis library (Col 1, Lines 9-13); and

comprising connection information and delay time information for a plurality of circuits (Col 1, Lines 39-40; Col 1, Lines 60-62; Col 1, Lines 45-48).

BL does not expressly teach that for at least one of the plurality of circuits, the library further comprises logical operation information. **HAS** teaches that for at least one of the plurality of circuits, the library further comprises logical operation information (Col 1, Lines 58-61 and Col 2, Lines 31-35), as delay verification time can be shortened and high speed delay

verification achieved by calculating delay time based on logic information, connecting information and delay information (Col 2, Lines 28-35). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **BL** with the system of **HAS** that included for at least one of the plurality of circuits, the library further comprising logical operation information, as delay verification time could be shortened and high speed delay verification achieved by calculating delay time based on logic information, connecting information and delay information.

BL does not expressly teach the logical operation information representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit. **HS** teaches the logical operation information representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit (Fig. 3; Col 1, Lines 28-35; Col 2, Lines 30-42; Col 3, Lines 12-16; Col 4, Lines 12-15), as this provides correct delay time even when either of rise or fall of the signal has no effect in a delay time computation process (Col 2, Lines 61-65). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **BL** with the system of **HS** that included the logical operation information representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit, as this would provide correct delay time even when either of rise or fall of the signal had no effect in a delay time computation process.

BL does not expressly teach that the delay information for the at least one circuit is based upon a logical state transition at an input terminal and its corresponding logical state transition at an output terminal as represented by the logical operation information for the at least one circuit; and when making a delay analysis of the logic circuit comprising the at least one circuit, a delay time is selected from the delay time information according to the type of logical state transitions present at selected input and output terminals of the at least one circuit. **HS** teaches that the delay information for the at least one circuit is based upon a logical state transition at an input terminal and its corresponding logical state transition at an output terminal as represented by the logical operation information for the at least one circuit; and when making a delay analysis of the logic circuit comprising the at least one circuit, a delay time is selected from the delay time information according to the type of logical state transitions present at selected input and output terminals of the at least one circuit (Col 2, Lines 30-42; Col 3, Lines 5-26; Col 3, Lines 12-16; Col 4, Lines 12-15), as this provides correct delay time even when either of rise or fall of the signal has no effect in a delay time computation process (Col 2, Lines 61-65). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **BL** with the system of **HS** that included the delay information for the at least one circuit being based upon a logical state transition at an input terminal and its corresponding logical state transition at an output terminal as represented by the logical operation information for the at least one circuit; and when making a delay analysis of the logic circuit comprising the at least one circuit, a delay time was selected from the delay time information according to the type of logical state transitions present at selected input and output terminals of the at least one

circuit, as this would provide correct delay time even when either of rise or fall of the signal had no effect in a delay time computation process.

Per Claim 4:

BL teaches a computer-readable medium having stored thereon a program for executing a process step (Col 2, Lines 42-50).

BL does not expressly teach a computer-readable medium having stored thereon a program for executing a process step of performing a delay calculation using selected delay time as a propagation delay time of at least one circuit. **HS** teaches a computer-readable medium having stored thereon a program for executing a process step of performing a delay calculation using selected delay time as a propagation delay time of at least one circuit (Col 3, Lines 5-26), as this provides correct delay time even when either of rise or fall of the signal has no effect in a delay time computation process (Col 2, Lines 61-65). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the computer-readable medium having stored thereon a program of **BL** with the computer-readable medium having stored thereon a program of **HS** that included executing a process step of performing a delay calculation using selected delay time as a propagation delay time of at least one circuit, as this would provide correct delay time even when either of rise or fall of the signal had no effect in a delay time computation process.

Arguments

7.1 As per the applicant's argument that "the combination of Blinne et al., Hasegawa '168 and Hasegawa '511 fails to teach or suggest a delay analysis library comprising delay information for a circuit that is based upon the logical state transitions at the input and output terminals of a logical circuit where the delay analysis library stores the delay information based on the correspondence between the input terminal logic state transitions and the output terminal logic state transitions; the combination of Blinne et al., Hasegawa '168 and Hasegawa '511 does not use input terminal logic state transitions, the output terminal logic state transitions and the delay information in the same manner as the present invention", the examiner respectfully disagrees. **HS** teaches a delay analysis library comprising delay information for a circuit that is based upon the logical state transitions at the input and output terminals of a logical circuit where the delay analysis library stores the delay information based on the correspondence between the input terminal logic state transitions and the output terminal logic state transitions; HS uses input terminal logic state transitions, the output terminal logic state transitions and the delay information in the same manner as the present invention (Col 3, Lines 12-16; Col 4, Lines 12-15).

7.2 As per the applicant's argument that "Blinne et al. ignore the logical operation of the analyzed logic circuit by independently recording each of the many inputs of the logic circuit ... Blinne et al. uses the delay time of the input with the longest delay time; this delay time is longer than what would be found in normal AND gate operation, because in that case, the output falls as soon as the input with the shortest time falls", the applicant's attention is directed to **HAS** and **HS** as shown in Paragraph 6.1 above. **HAS** teaches that the library comprises logical operation

information (Col 1, Lines 58-61 and Col 2, Lines 31-35). **HS** teaches the logical operation information representing correspondence between logical state transitions at each input terminal of the circuit and logical state transitions at each output terminal of the circuit (Fig. 3; Col 1, Lines 28-35; Col 2, Lines 30-42; Col 3, Lines 12-16; Col 4, Lines 12-15). In Fig 2, if the OR gate is replaced by an AND gate, a signal transition result for the AND gate can be obtained using the same principle as shown in Fig 3. Then it would be found in normal AND gate operation the output falls as soon as the input with the shortest time falls.

7.3 As per the applicant's argument that "while the circuit modeling technique disclosed by Hasegawa'511 uses the rising and falling signals, it still rely upon the maximum delay times, stored in the arc between nodes, for the propagation delay time calculation ... Hasegawa'511 does not teach or suggest determining delay time based on the logical state transitions at the input and output terminals ... so that the rising edge signals and the falling edge signals use the same estimated delay time for delay calculations", the examiner respectfully disagrees. **HS** teaches the logical operation information representing correspondence between logical state transitions at each input terminal of circuit and logical state transitions at each output terminal of the circuit; **HS** teaches determining delay time based on the logical state transitions at the input and output terminals, so that the rising edge signals and the falling edge signals do not use the same estimated delay time for delay calculations (Fig. 3; Col 1, Lines 28-35; Col 2, Lines 30-42; Col 3, Lines 12-16; Col 4, Lines 12-15).

Conclusion

ACTION IS FINAL

8. Applicant's arguments with respect to claim rejections under 35 USC 103 (a) are not persuasive. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 703-305-0043. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska, can be reached on (703) 305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

K. Thangavelu
Art Unit 2123
March 30, 2004